APPLICATION NOTE AN199

Using the SL6609A Direct Conversion Pager Receiver

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This application note outlines a basic circuit for the SL6609A Direct Conversion Pager Receiver for use in standard paging applications at 153MHz, 282MHz and 450MHz. Fig. 1 is a block diagram of the SL6609A, showing the pin allocation and the internal structure of the device. Table 1 gives detailed descriptions of these functions.

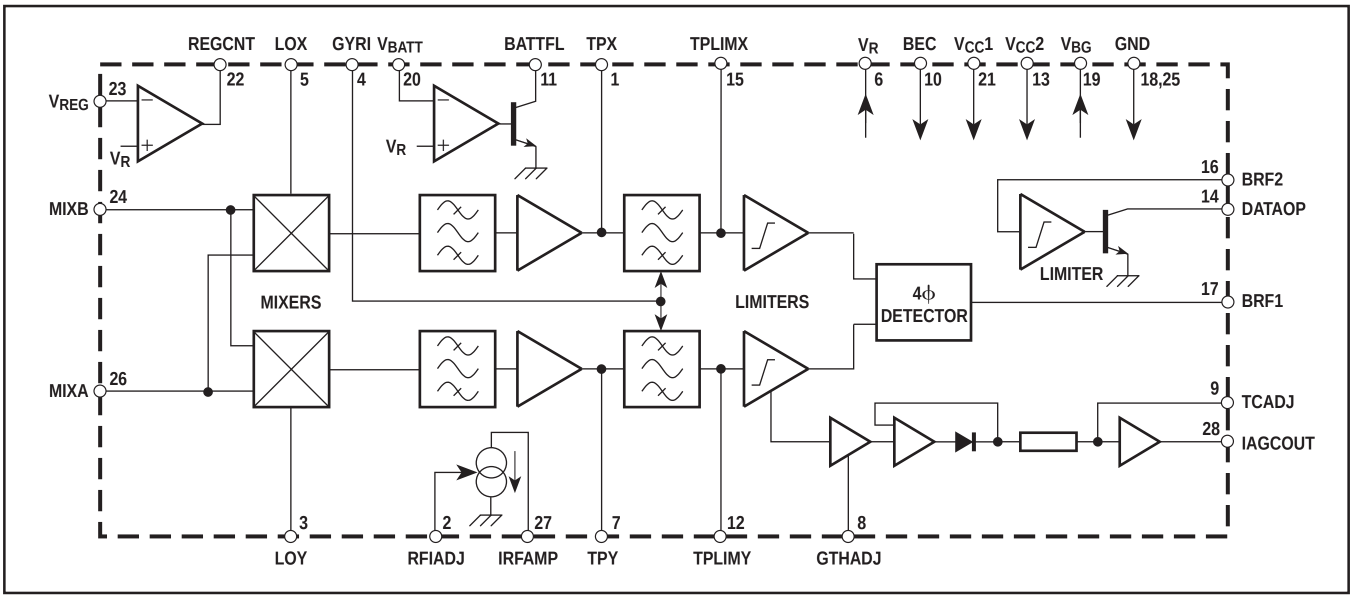

Fig. 1 SL6609A internal block diagram

Pin	Name	Description
1	TPX	**Channel X test point.** Channel X internal amplifier output/gyrator filter input. This pin is used to measure the receiver signal level during receiver set up. It may also be used in conjunction with pin 15 (TPLIMX) to measure the response of the gyrator filters. It can be used to add additional filtering in the channel in the form of an additional external capacitor.
2	RFIADJ	**Current source adjust.** Pin 2 allows adjustment of the current source which is designed for use with the external RF amplifier. See **CIRCUIT FACILITIES.**
3	LOY	**Mixer LO input.** The local oscillator signal is applied to pin 3 in phase quadrature to pin 5. For the phase quadrature circuit see RF Amplifier and Local Oscillator Network. The LO input of the mixers require a bias path to $V_{CC}1$ (see R5 and R6 on the Applications Circuit, Fig. 2).
4	GYRI	**Gyrator filter adjust.** The bandwidth of the on-chip gyrator filter can be adjusted using a resistor from pin 4 to GND. For values see **Setup for Optimum Performance.**
5	LOX	**Mixer LO input.** See pin 3
6	V_R	**Voltage reference, V_R.** 1V internal reference voltage. It may be used for the bias of external RF amplifier and LO Circuits. It is also a reference for pins 1,7,8 and 9.
7	TPY	**Channel Y.** Channel Y internal amplifier output/gyrator filter input. This pin is used to measure the received signal level during receiver set up. It may also be used in conjunction with pin 12 (TPLIMY) to measure the response of the gyrator filters. It can be used to add additional filtering in the channel in the form of an additional external capacitor.

Table 1 Pin descriptions

Cont…

Pin	Name	Description
8	GTHADJ	**Audio AGC level adjust.** Level adjustment for the external AGC drive. See Fig. 5. The voltage at pin 8 is dictated by an external resistor (R16 in Applications Circuit) and an internal current source driven by the wanted audio (baseband) signal level. With no signal output to the receiver, the output of current source 1 tends to be zero and so the voltage at pin 8 is V_R. This gives the result that the output of current source 2 (pin 28) tends to 0µA. (i.e. the AGC is disabled). With a signal incident on the receiver, current source 1 driving pin 8 is turned on and there is a voltage drop across the external resistor (R16). The value of R16 dictates the voltage drop and hence the sensitivity of the AGC circuit. For a value of R16, see Fig. 2.
9	TCADJ	**Audio AGC time constant.** The attack (turn on) and decay (duration) times of the Audio AGC are set by an RC network connected to pin 9. See Fig. 2 for details.
10	BEC	**Battery economy.** The battery economy facility allows the device to be powered down by pulling pin 10 to GND. If not required this should be connected to $V_{CC}2$.
11	BATTFL	**Low battery flag output.** The battery flag is the output of an on-chip comparator with VR as the reference voltage. When V_{BATT} (pin 20) $<$ V_R, Battery Flag output is low. BATTFL is an open collector output.
12	TPLIMY	**Channel Y gyrator filter output.** See pin 7. Pin 12 provides a monitor of the gyrator filter output of channel Y to enable the response of the filter to be accurately measured and adjusted using pin 4. For details refer to **Setup for Optimum Performance.**
13	$V_{CC}2$	**$V_{CC}2$ supply.** This pin requires adequate audio decoupling to GND. If a DC-DC converter is used to generate this voltage care must be taken to prevent power supply noise reducing the sensitivity of the device.
14	DATAOP	**Data output.** Open collector data output. This requires a pull-up resistor to a suitable voltage reference e.g. $V_{CC}2$.
15	TPLIMX	**Channel X gyrator filter output.** See pin 1. Pin 15 provides a monitor of the gyrator filter output of channel X, to enable the response of the filter to be accurately measured and adjusted using Pin 4. For details refer to **Setup for Optimum Performance.**
16	BRF2	**Data buffer input.** Input to the data limiter. This pin is normally connected directly to Pin 17.
17	BRF1	**Output of the phase detector.** For optimum performance a Bit Rate filter can be applied to this pin. This is achieved by connecting a capacitor between Pin 17 and GND. The value of this capacitor is dependent on the data rate. For the value of this capacitor see **Setup for Optimum Performance.**
18	DIGGND	**Digital ground.** This is the ground for the digital circuits in the receiver.
19	V_{BG}	**Bandgap voltage reference (1·2V).** This may be used to bias an external RF amplifier. See **APPLICATION CIRCUIT REQUIREMENTS** for details.
20	V_{BATT}	**Battery flag input.** Connect this pin to Pin 21 ($V_{CC}1$) if a 1V threshold is required. Alternative thresholds may be determined using an external potential divider. See **APPLICATION CIRCUIT REQUIREMENTS** for details.
21	$V_{CC}1$	**$V_{CC}1$ supply.** This requires adequate audio and RF decoupling if optimum device sensitivity is to be achieved.
22	REGCNT	**Voltage regulator control output.** 1V on-chip voltage regulator output, used to drive a suitable PNP transistor. See **Setup for Optimum Performance**. For stability purposes a capacitor should be applied between Pin 22 and Pin 23. The regulator is only specified for $V_{CC}1 \geqslant 1{\cdot}1V$.
23	V_{REG}	**Voltage regulator sense.** This should be connected to the load of the regulator. If the regulator is not required, and no active components are connected to Pin 22 and Pin 23, then Pin 23 should be connected to Vcc2.
24	MIXB	**Mixer RF input B.** Input to the device from an external RF amplifier. The signal should be applied differentially between Pin 24 and Pin 26. The differential signal to the mixers may be DC coupled if no DC voltage is applied, otherwise AC coupling should be used.

Table 1 Pin descriptions (continued)

Cont…

Pin	Name	Description
25	GND	**Receiver ground.** Ground for receiver RF circuits.
26	MIXA	**Mixer RF input A.** Differential input from an external RF amplifier. See pin 24.
27	IRFAMP	**Current source output IRF.** An on chip current source for use in RF amplifier designs. This allows the current in the RF amplifier to be independent of supply voltages. See **APPLICATION CIRCUIT REQUIREMENTS** for details. It is very important to use the current source with the RF amplifier. The current source incorporates an RF signal AGC. This ensures optimum operation of the device for high input signal levels.
28	IAGCOUT	**Audio AGC output current.** See Fig. 5. A current source controlled by the Audio signal level and the AGC threshold adjust (pin 8). The current source is intended to sink current from an PIN diode on the RF input and hence reduce the RF signal incident on the RF amplifier input.

Table 1 Pin descriptions (continued)

APPLICATION CIRCUIT REQUIREMENTS

The example application circuit is shown in Fig. 2. To achieve optimum performance of the device it is necessary to incorporate a low noise RF amplifier at the front end of the receiver. This is easily biased using the on-chip facilities provided. The receiver also requires a local oscillator input at the wanted channel frequency.

RF Amplifier and Local Oscillator Network

The design of the RF amplifier is simplified by the on-chip current source and the two voltage references V_{BG} and V_R.

A suitable circuit is shown in Fig. 3. The current through the load and hence the gain of the amplifier is controlled by the on-chip current source IRF. This ensures that the gain of the amplifier is independent of the supply voltage. Also, as V_R and V_{BG} are independent of supply voltage, it ensures that the bias points of the transistors are also stable and independent of supply voltage, with each transistor simply biased via a series resistor to the appropriate voltage reference.

The RF amplifier current source (pin 27) may be adjusted with the use of an external resistor connected between pin 2 and a voltage reference or ground. For details see **RF Current Source Adjustment**. Also, the RF amplifier current source forms part of the RF AGC circuitry, reducing the RF amplifier current if excessive signal is incident on the mixer inputs. It is very important to use the current source in the design of the RF amplifier. This ensures that the SL6609A will operate with high level input signals.

The differential input required by the mixers is applied from the RF amplifier via a suitable transformer (T1). This forms a tuned load with the variable capacitor (VC1). This load is tuned to the operating frequency of the device. The normal operating gain of the RF amplifier is also controlled by the load resistor R13 in parallel with the transformer.

The input to the amplifier is an LC network (C26, L1 and C27) designed for optimum noise figure of the RF amplifier in order to give best overall device sensitivity.

For optimum sensitivity, adjacent channel and third order intermodulation performance refer to **Setup for Optimum Performance** for the gain distribution requirements of the receiver chain.

The local oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at their −3dB/45° transfer characteristic at the local oscillator frequency, giving a full 90° phase differential between the LO ports of the device (see Fig. 4). Each LO port also requires an equal level of drive from the oscillator. In this application circuit the local oscillator is supplied by a signal generator with a source impedance of 50Ω hence the total RC network (including mixer bias) is designed to have this input impedance.

Note: All voltage and current sources used for bias of the RF amplifier and receiver mixers should be decoupled at RF and audio frequencies using suitable capacitors. RF decoupling should be done as close as possible to the RF circuit.

RF Amplifier to Mixer Transformerless Matching

An LC coupling network can be used to replace the transformer T1 in the applications circuit, Fig. 2. This couples the RF amplifier output to the SL6609A mixer inputs MIXA (pin 26) and MIXB (pin 24). The circuit is shown in Fig. 10.

Regulator Requirements

The on-chip regulator must be used in conjunction with a suitable PNP transistor to achieve reliable regulation. As the transistor forms part of the regulator feedback loop, the transistor should exhibit the following characteristics:

$$H_{FE} \geqslant 100 \text{ for } V_{CE} \geqslant 0.1\text{V}$$

A suitable transistor (TR1) is specified in Fig. 2 and Table 2.

RF and Audio Decoupling Requirements

All voltages and references should be adequately decoupled at audio (baseband) frequencies. Also, where a voltage reference or current source is used to bias the RF or LO circuits it is necessary to apply RF decoupling to the supply at the point of connection.

Open Collector Outputs

The Data Output and the Battery Flag output are open collector and require a pull up resistor to a suitable voltage reference. Care must be taken to ensure that the pull up resistor is adequate to supply sufficient current to the load.

CIRCUIT FACILITIES

Audio AGC Circuit

Fig. 5 shows the internal structure associated with the Audio AGC facility. It consists of a current sink which is controlled by the audio (baseband) signal amplitude. It has three parameters that may be controlled by the user; the attack (turn on) time, decay (duration) time and threshold level.

Attack time

The attack time is simply determined by the value of the external capacitor connected to pin 9 (TCADJ). The external capacitor is in series with an internal 100kΩ resistor and the time constant of this circuit dictates the attack time of he AGC i.e. $T_{ATTACK} \propto 100k \times C_{TC}$ (C8)

Decay time

The decay time is determined by the external resistor R9 (R_{DECAY}) connected in parallel to the capacitor C8. The decay time is simply $T_{DECAY} = R9 \times C8$.

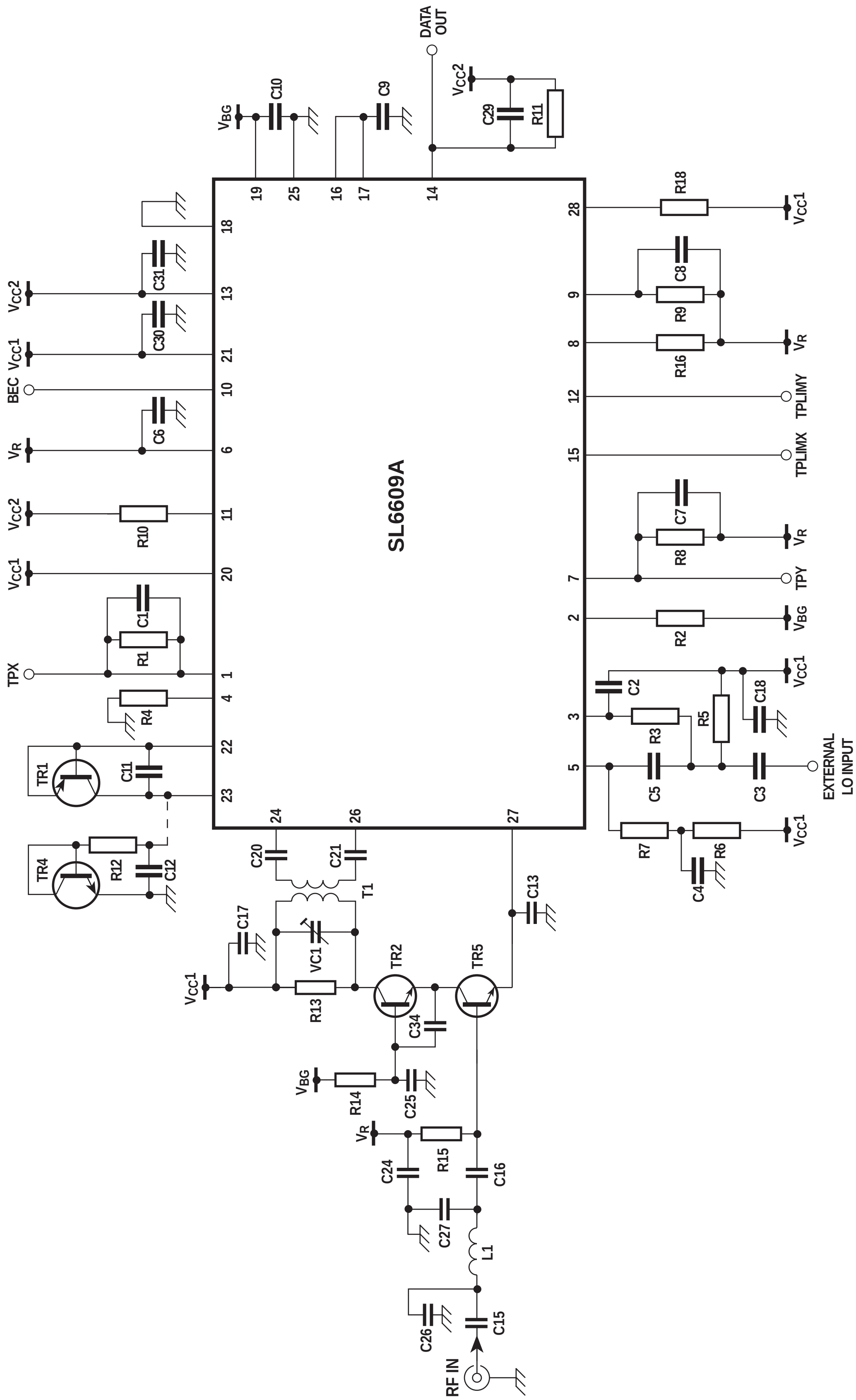

Fig. 2 Basic SL6609A application circuit (282MHz receiver), showing RF amplifier with external injected LO (no audio AGC)

Resistors		Capacitors		Capacitors (cont.)		Inductors	
R1	O/C	C1	1nF	C19	Not used	L1	68nH(4) (6)
R2	O/C	C2	5·6pF(4)	C20	1nF	T1	30nH 1:1, Coilcraft M1686-A
R3	100Ω	C3	1nF	C21	1nF	**Transistors**	
R4	100kΩ	C4	1nF	C22	Not used		
R5	100Ω	C5	5·6pF(4)	C23	Not used	TR1	Zetex FMMT58
R6	100Ω	C6	2·2µF	C24	1nF	TR2	Toshiba 2SC5065
R7	100Ω	C7	1nF	C25	1nF	TR3	Not used
R8	O/C	C8	100nF	C26	6·8pF(4) (6)	TR4	Philips BFT25A(2)
R9	220kΩ	C9	2nF(5)	C27	O/C(4) (6)	TR5	Toshiba 2SC5065
R10	1MΩ	C10	2·2µF	C28	Not used		
R11	100kΩ(1)	C11	100nF	C29	100pF		
R12	330Ω(2)	C12	1nF	C30	2·2µF		
R13	Note(3)	C13	1nF	C31	2·2µF		
R14	4·7kΩ	C14	Not used	C34	2·2pF		
R15	4·7kΩ	C15	1nF	VC1	1-10pF		
R16	33kΩ	C16	1nF				
R17	Not used	C17	2·2µF				
R18	12kΩ	C18	1nF				

Table 2 Component list for 282MHz characterisation board (Fig. 2)

NOTES
1. The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.
2. R12 and TR4 form a dummy load for the regulator. Permitted load currents for the regulator are from 250µA to 3mA.
3. The value of R13 is determined by the set up procedure. See **Setup For Optimum Performance**.
4. The values of these components are dependent on the operating frequency.
5. The value of C9 is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.
6. L1 and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in Fig. 2 with no audio AGC connected. If the audio AGC circuit is connected, the values will require a small change to achieve a good match.
7. Values for R16, R8, C8 and R18 are included so that the open loop action of the AGC circuit can be observed. If this is not required, it can be disabled as described in the section **Disabling the audio AGC circuits**.

Threshold level

When a large audio (baseband) signal is incident on the input of the AGC circuit (Fig. 5), the variable current source is turned on. This causes a voltage drop across R16. The voltage potential between V_R and the voltage on pin 8 causes a current to flow from pin 9. This charges C8 through the 100kΩ internal resistor. As the voltage across the capacitor increases, current source 2 is turned on and this sinks current from pin 28.

The current sink on pin 28 can be used to drive the external AGC circuit by causing a PIN diode to conduct, reducing the signal to the RF amplifier.

The relationship between the incident audio signal and current source 1 is shown in Fig. 8. This can be used in conjunction with the value of R16 to set the voltage at pin 8 for any particular signal level.

The relationship between the voltage at pin 8 and the output of current source 2 is given in Fig. 9.

Using both figures, the value of R16 can be selected to give the required output current at pin 28 for any particular input signal level. Note, however, that the maximum audio signal and hence the audio AGC current (pin 28) is limited in practice by a typical receiver gain distribution to approximately 45µA.

Disabling the audio AGC circuits

The audio AGC may be simply disabled by connecting pin 8 (GTHADJ) to V_R. Alternatively the audio AGC may be disabled by connecting pin 28 (IAGCOUT) to $V_{CC}2$ and connecting pin 9 (TCADJ) directly to V_R (pin 6). This would then allow the use of the voltage drop across R16, when connected to pin 8, to be used as an RSSI (Received Signal Strength Indicator).

RF Current Source Adjustment

With pin 2 open circuit and with pin 27 connected to a potential of 0·2V (i.e. the emitter of a transistor with the base voltage V_B = 1V (i.e. V_R)), the current is nominally set to give IRF= 500µA.

The current source may be adjusted by connecting pin 2 via a suitable resistor to a voltage reference or ground.

The value of the resistor is determined by the required increase or decrease in IRF from the nominal 500µA. (i.e. pin 2 open circuit). The nominal voltage of pin 2 is 0·7V. To decrease IRF, connect pin 2 to ground using a resistor R, where

$$R = \frac{V - 0{\cdot}7V}{(500\mu A - I_{REQ})/5}$$

I_{REQ} = required IRF

To increase IRF, connect pin 2 to a voltage reference V (e.g. V_{BG}) using a resistor R, where

$$R = \frac{0{\cdot}7V}{(I_{REQ} - 500\mu A)/5}$$

NOTES
1. V_{BG} should not be used to sink current.
2. The on-chip voltage reference V_R should not be used as a reference for pin 2 as it is not capable of sourcing the required current.

On-Chip Voltage References

The on-chip voltage reference V_{BG} (1·2V) may be used to bias an external RF amplifier and as a reference for the on-chip RF AGC (see pin 2). V_{BG} can source a maximum current as specified in the device data sheet. V_{BG} should not be used to sink current.

The on-chip voltage references V_R (1·0V) may be used to bias an external RF amplifier and as a reference for pins 1,7,8 and 9. V_R can source or sink a maximum current as specified in the SL6609A data sheet.

Battery Flag Input

The battery flag threshold may be simply increased by using a suitable potential divider so that at the required battery threshold voltage, the voltage at pin 20 (V_{BATT}) is 1V.

Setup for Optimum Performance

To obtain optimum receiver sensitivity it is necessary to have a Low Noise RF Amplifier at the front end of the receiver (see **RF Amplifier and Local Oscillator Network**). However, to achieve optimum third order intermodulation rejection it is essential to ensure that the amplifier gain is not greater than the value necessary to achieve good sensitivity. Similarly, to achieve optimum adjacent channel rejection it is necessary to limit the internal gain of the device to that required to obtain sensitivity. Increasing the internal or the RF Amplifier gain beyond these points will degrade the receiver performance.

The procedure outlined here represents a method of obtaining optimum performance under the following operating conditions:

Frequency of Operation	282MHz
Deviation Frequency	4kHz
Local Oscillator Input Power	−15dBm (50Ω source impedance, see Fig. 4)
Power Supply $V_{CC}1$	1·3V
Power Supply $V_{CC}2$	2·7V
Nominal Gyrator pin 4	100kΩ
R1	Open Circuit
R8	Open Circuit
C1-C7	1nF

If the proposed frequency of operation is different to that stated above, the signal levels stated should be used as a guide to obtaining the optimum gain distribution within the receiver and RF amplifier.

Note: The following set up procedure was undertaken using the RF Amplifier specified in Fig. 2 and should only be used as guidance if alternative RF amplifiers are proposed.

Having obtained the component values for optimum performance for a specified RF amplifier, circuit layout, and operating conditions then, provided the RF amplifier design is not device dependent, it should not be necessary to undertake the set up procedure for each individual circuit.

The local oscillator drive level and receiver gain used can be optimised if required by the user to trade off sensitivity with the receiver interferer performance (i.e. IP3). The receiver gain level specified below is considered adequate to achieve a good balance between sensitivity and receiver interferer performance.

Sensitivity can be increased, to the detriment of receiver interferer performance, by increasing the LNA gain. Fig. 11 and Fig. 12 show typical trends.

Increasing the local oscillator drive level, while reducing the LNA gain to keep the same gain to the receiver test points (TPX and TPY), can be used to increase the receiver interferer performance whilst maintaining a near constant sensitivity level. This is typically true for local oscillator signals in the range 10mVrms to 50mVrms as measured at the receiver local oscillator inputs pins LOX and LOY.

Set up procedure

If the Audio AGC function of the SL6609A is being used in a particular application it must be disabled before undertaking the following steps. To disable the audio AGC function connect GTHADJ directly to V_R, leaving all existing circuitry connected to GTHADJ and V_R unaltered.

(a) Apply a signal with a frequency of $f_{LO}+4$kHz, −73dBm, with no modulation on, to the input of the RF amplifier.
(b) Monitor test point TPX (pin 1) with an oscilloscope. Determine that the signal is at a frequency of 4kHz. Adjust the LO or RF frequency to achieve this. Adjust VC1 on the RF amplifier load until the 4kHz signal level is maximum. This should be >200mV p-p. Note: If the level of the signal is above 260mV p-p the signal will not be sinusoidal due to the saturation of the receiver.
(c) Use the parallel load resistor (R13) on the RF amplifier to reduce the gain of the RF amplifier to obtain a level of 160mV 10mV p-p at TPX. Ensure that the signal at TPY (pin 7) is also at a level within 10mV of that at TPX (pin 1). Typically, R13 will be:

1·2kΩ for 153MHz
1·8kΩ for 282MHz
3·9kΩ for 470MHz

(d) Connect a capacitor between pin 16 and GND in accordance with Table 3.

Data rate (bps)	Capacitor required
512	2nF
1200	1nF
2400	470pF

Table 3

Fine adjustment of the gyrator filter

Due to the tolerance of the manufacturing process the gyrator response may vary by 15% for a given value of resistor connected between pin 4 and GND. For accurate alignment the filter will require adjustment. This is simply achieved by undertaking the following procedure: Note: For the following levels to apply the procedure below should follow Setup for Optimum Performance.

(a) Set the input RF frequency to $f_{LO}+4$kHz, no modulation.
(b) Monitor the signal at the test point TPX (pin 1). Check that the signal frequency is 4kHz. Adjust the LO or RF frequency to obtain this. Adjust the RF signal input until a level of 4mV p-p is measured.
(c) Monitor the test point TPLIMX (pin 15) and note the peak to peak signal level; this should be approximately 170mV p-p but not limiting.
(d) Adjust the RF signal generator frequency until the signal level drops to 70·8% (−3dB) of the level noted in step (c).
(e) Note the frequency of the RF signal generator. The difference between the LO frequency and the RF input frequency represents the −3dB response of the filter.

Using a 100kΩ resistor to set the gyrator filters will give a nominal −3dB cut of 7·5kHz. Changing this resistor value causes a linear change in the frequency of the filter cutoff. For example, if a 100kΩ resistor results in a filter −3dB cut off equal to 7.5kHz then a 136kΩ resistor will give a 5·5kHz −3dB cutoff.

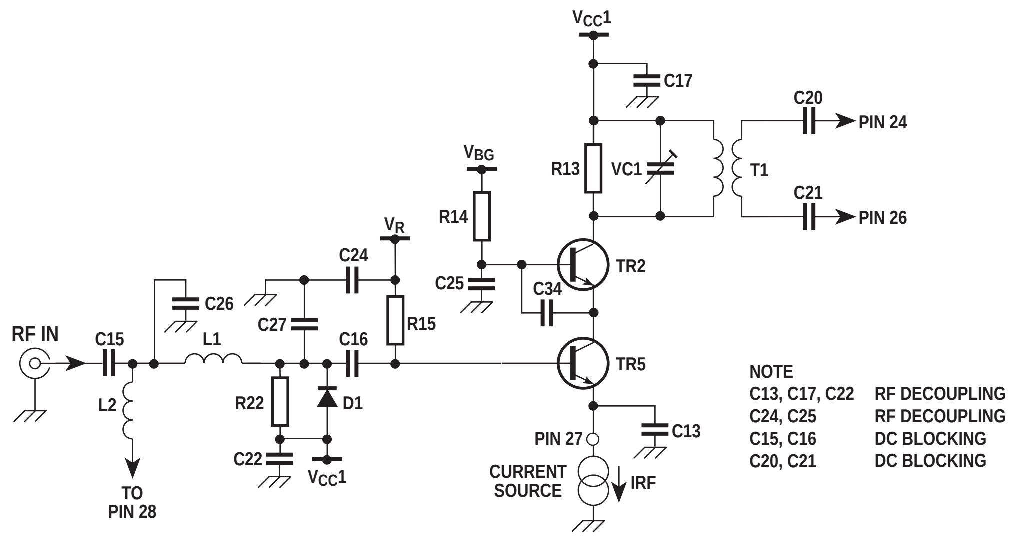

Fig. 3 RF amplifier

Component	Value
R13	Note(1)
R14	4·7kΩ
R15	4·7kΩ
R16	33kΩ
R22	47kΩ
C13	1nF
C15	1nF
C16	1nF
C17	1nF
C20	1nF(2)
C21	1nF(2)
C24	1nF
C25	1nF
L2	820nH
D1	MA862 (Panasonic)

Table 4a RF amplifier component values (non-frequency dependent)

NOTES
1. The value of R13 is determined by the setup procedure. See **Setup For Optimum Performance.**
2. C20 and C21 are purely for demonstration purposes. Pin 24 and pin 26 may be DC coupled provided that no DC voltage is applied to the mixer inputs.

Component	153MHz	280MHz	450MHz
C26	Not used	6·8pF	Not used
C27	Not used	Not used	Not used
C34	3·3pF	2·2pF	1·5pF
L1	150nH	68nH	39nH
T1	100nH Coilcraft N2261-A	30nH Coilcraft M1686-A	16nH Coilcraft Q4123-A
VC1	1-10pF	1-10pF	1-3pF
TR4, TR5	Toshiba 2SC5065	Toshiba 2SC5065	Philips BFT25A

Table 4b RF amplifier component values (frequency dependent). See also LO drive network, Fig. 4

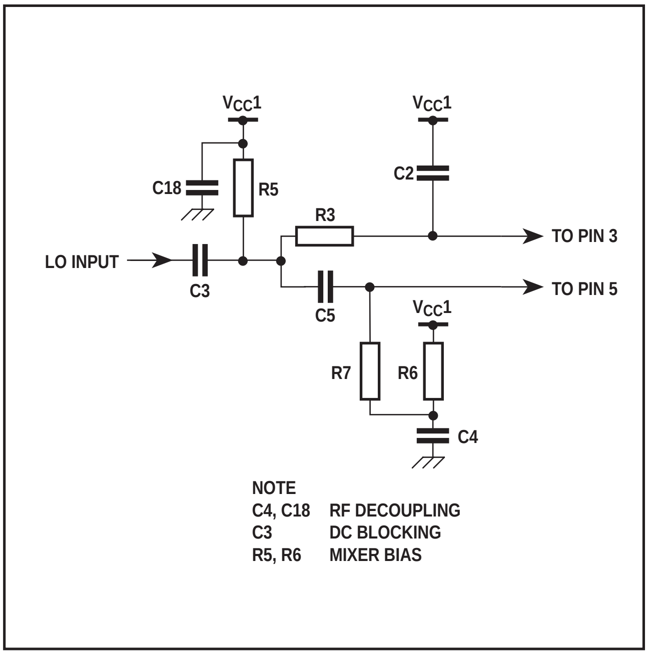

Fig. 4 Local oscillator drive network

Component	153MHz	280MHz	450MHz
C2	10pF	5·6pF	3·3pF
C5	10pF	5·6pF	3·9pF
C3,C4,C18	1nF, all frequencies		
R3,R5,R6,R7	100Ω, all frequencies		

Table 5 LO drive network component values for 50Ω input impedance (external LO injection)

Component	153MHz	280MHz	450MHz
C2	10pF	5·6pF	3·3pF
C5	10pF	5·6pF	3·9pF
R3	100Ω	100Ω	100Ω
R7	100Ω	100Ω	100Ω
C3	Set by load allowable on crystal osc. (4·7pF typ.)		
R5,R6	1kΩ, all frequencies		
C4,C18	1nF, all frequencies		

Table 6 LO drive network component values for high input impedance (crystal oscillator input)

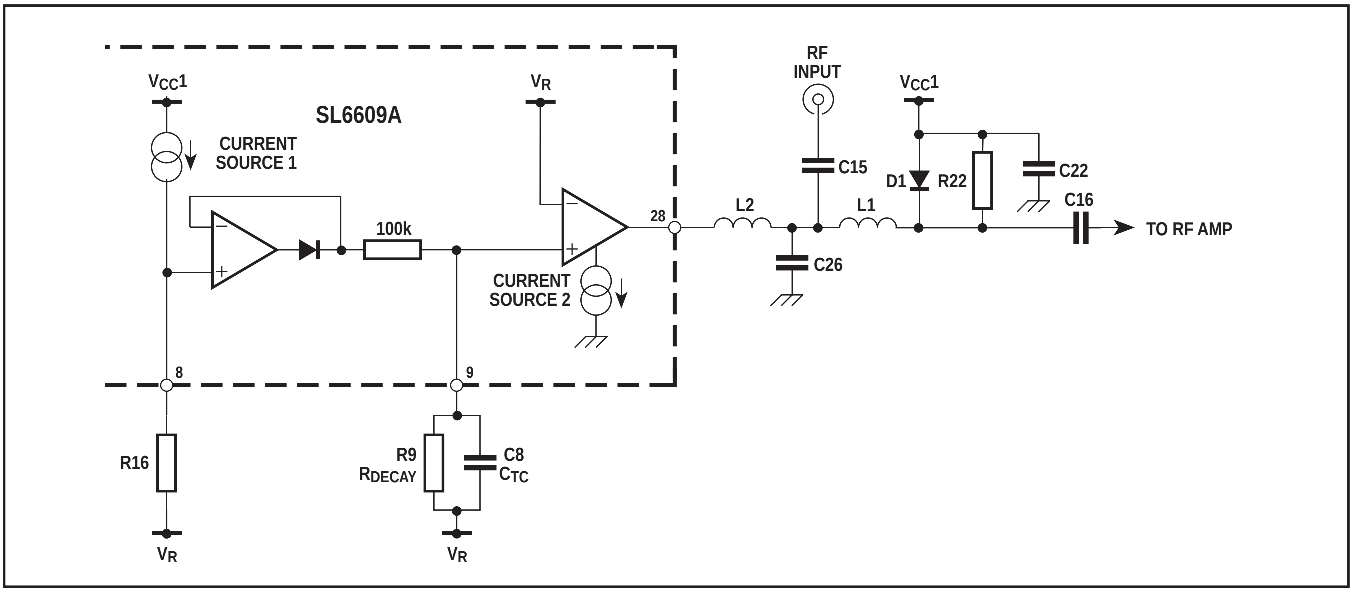

Fig. 5 AGC schematic

Resistors		Capacitors		Miscellaneous	
R9	220kΩ	C8	100nF(1)	L1	47nH(2)
R15	4·7kΩ	C15	1nF(2)	L2	820nH
R16	33kΩ(1)	C16	1nF	D1	MA862 (Panasonic)
R17	2kΩ	C22	1nF		
R22	47kΩ	C26	4·7pF(2)		
		C30	1nF		

Table 7 AGC component values (282MHz RF amplifier)

NOTES
1. R16 sets the gain (sensitivity) of the audio AGC. If R16 is increased then the the audio AGC will become active for a lower wanted signal level. Increasing R16 can cause the audio AGC loop to become unstable. C8 should be increased to increase the turn on/off time to prevent oscillation occuring.
2. L1, C15 and C26 are part of the RF amplifier (see Fig. 3).

AGC Response

Fig. 6 shows a typical AGC response with wanted and unwanted rejection level. If the AGC is required to become active earlier, it is possible to use the circuit shown in Fig. 7 to replace R16. However, it should be noted that the AGC has a fixed dynamic range.

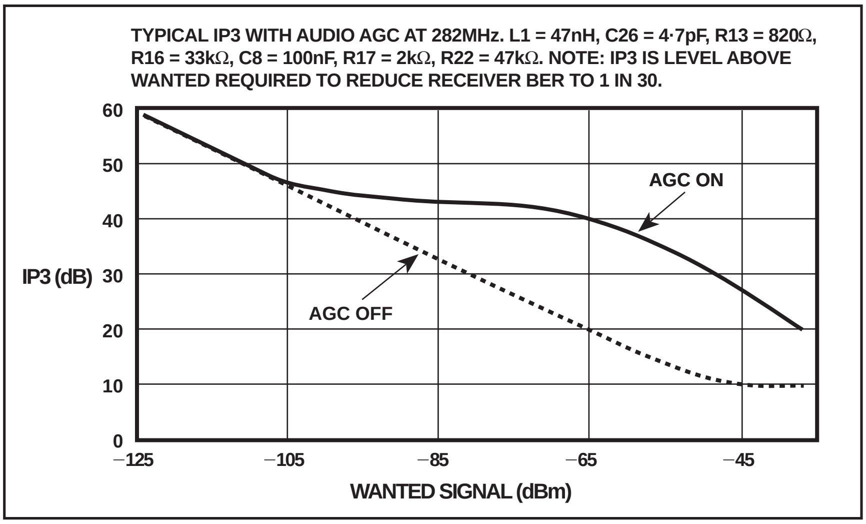

Fig. 6

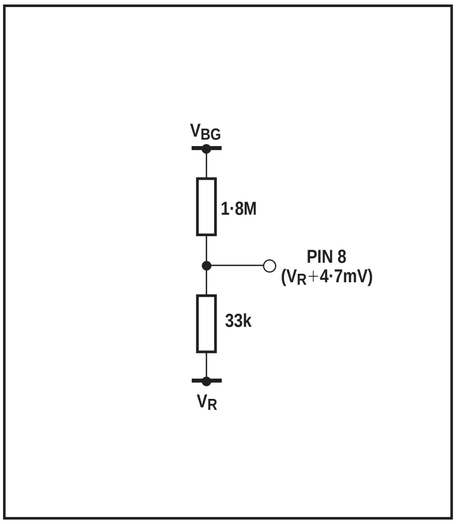

Fig. 7

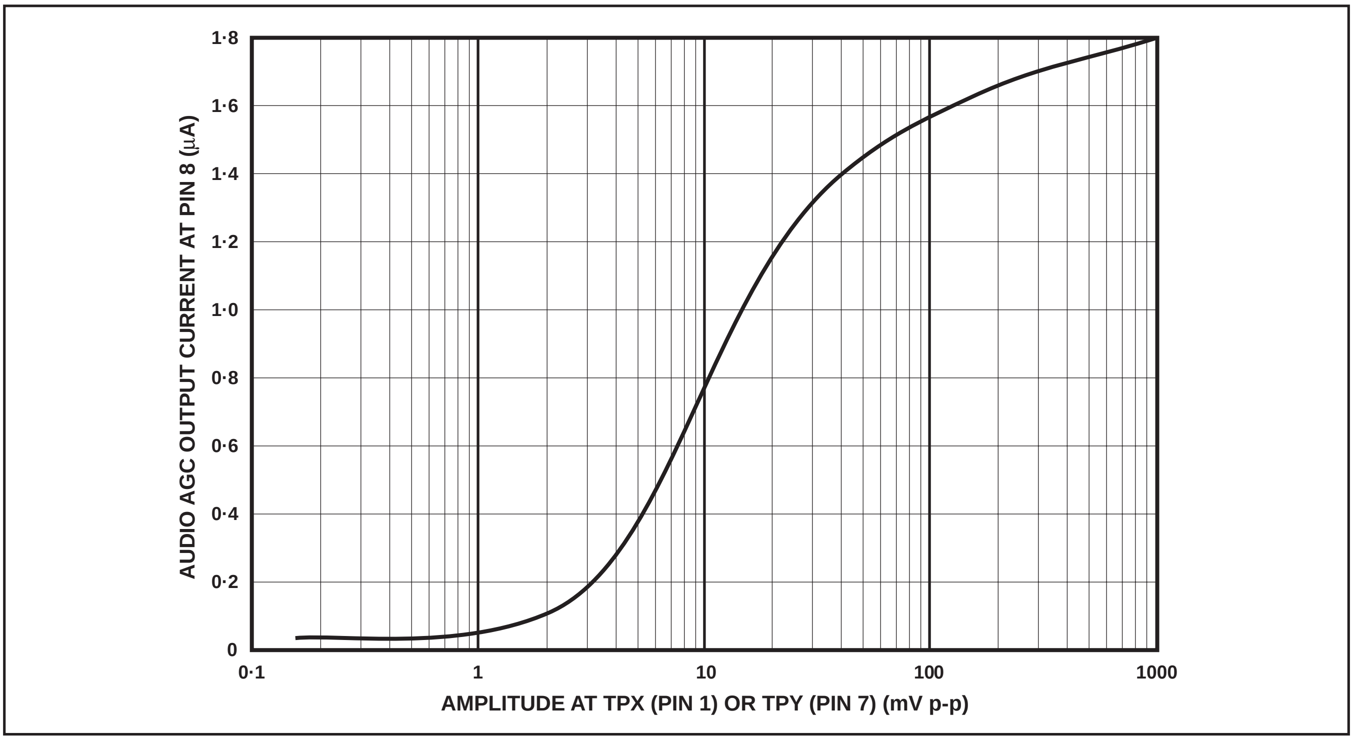

Fig. 8 RSSI audio AGC v. signal level at TPX or TPY

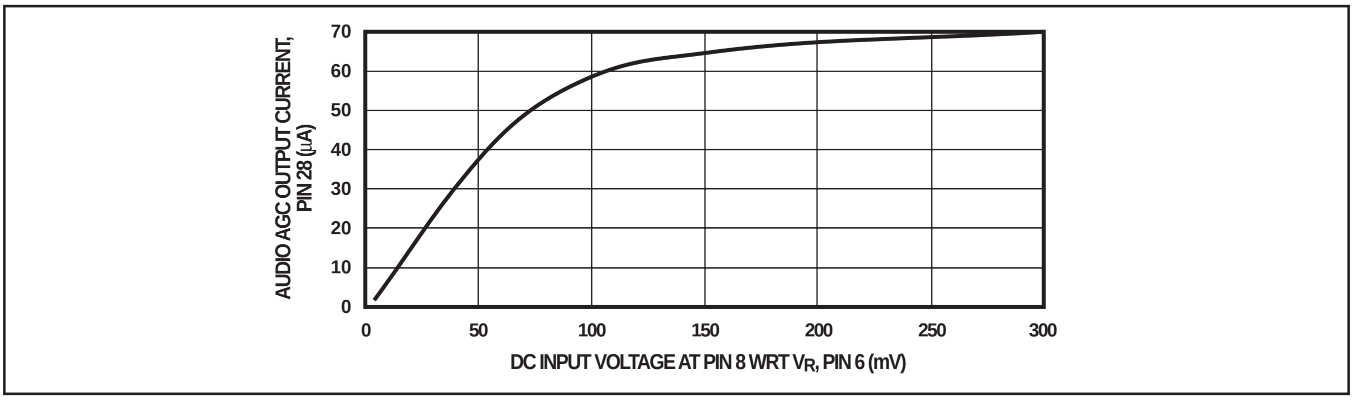

Fig. 9 Audio output current at pin 28 v. DC voltage at pin 8 (GTHADJ)

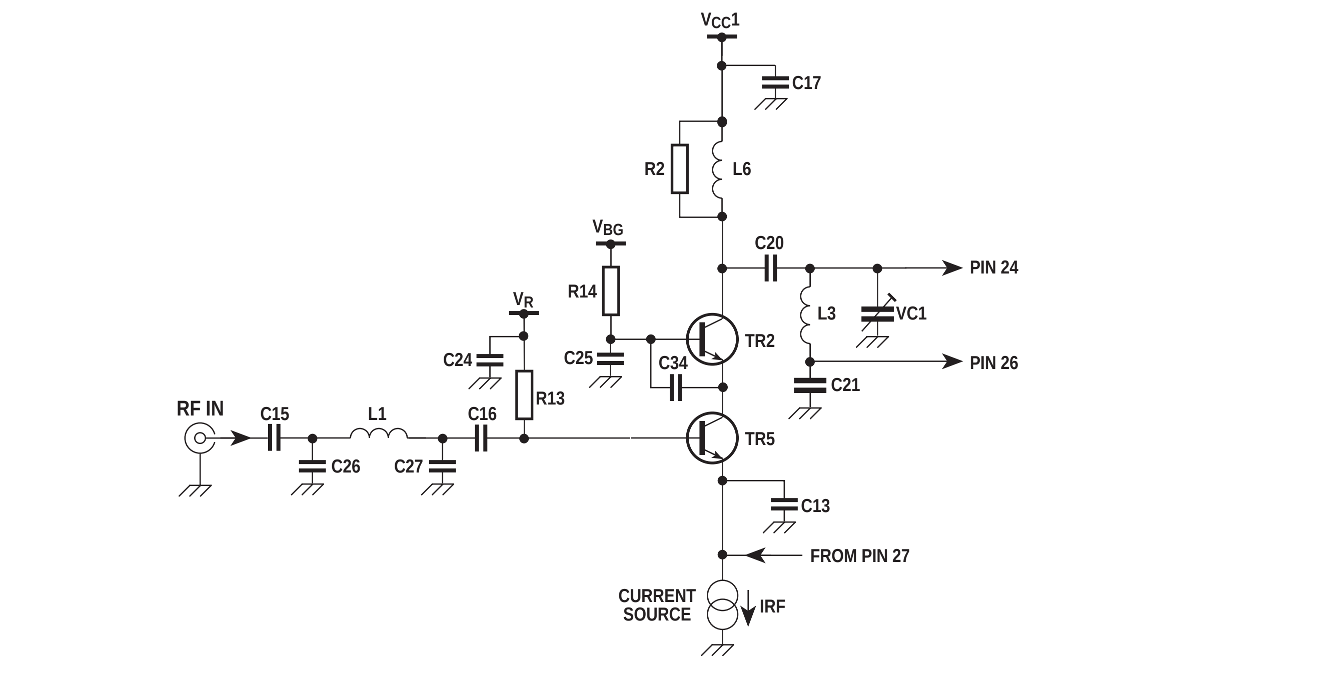

Fig. 10 RF amplifier with transformerless mixer matching circuit

Resistors		Capacitors	
R2	Note(1)	C13	1nF
R13	4·7kΩ	C15	1nF
R14	4·7kΩ	C16	1nF
		C24	1nF

Table 8a Component values for Fig. 10 (non-frequency dependent)

NOTES
1. The value of R2 is determined by the setup procedure. See **Setup For Optimum Performance.**

Component	153MHz	280MHz	450MHz
C20	1nF	1nF	1nF
C21	2·7pF	3·3pF	1pF
C26	Not used	6·8pF	Not used
C27	Not used	Not used	Not used
C34	3·3pF	2·2pF	1·5pF
L1	150nH	68nH	39nH
L3	330nH	100nH	39nH
L6	150nH	83nH	47nH
VC1	1-10pF	1-5pF	Not used
TR4, TR5	Toshiba 2SC5065	Toshiba 2SC5065	Philips BFT25A

Table 8b Component values for Fig. 10 (frequency dependent).

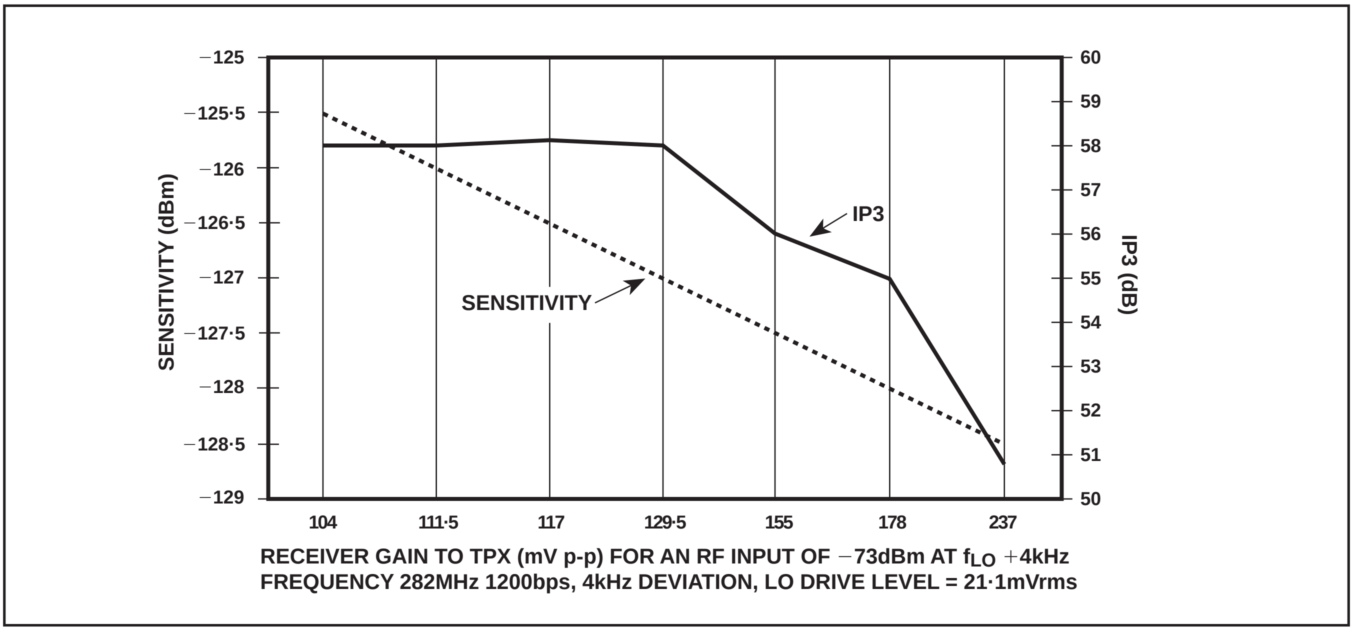

Fig. 11 Sensitivity, IP3 v. receiver gain

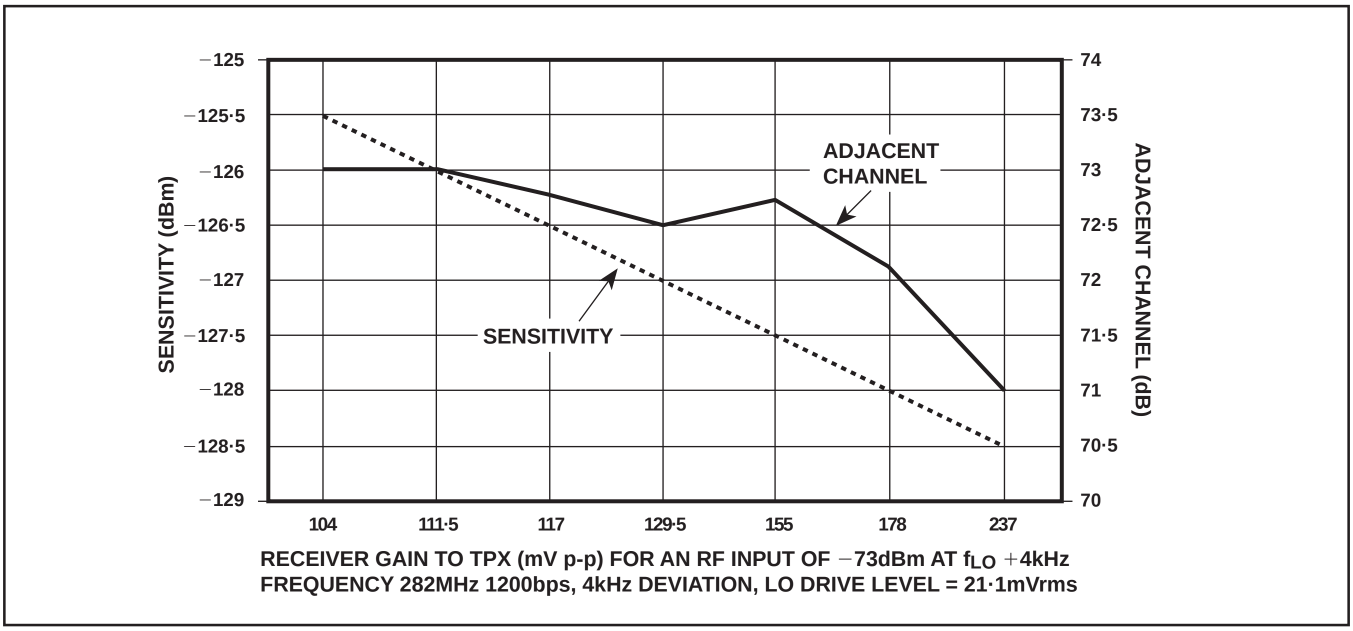

Fig. 12 Sensitivity, adjacent channel v. receiver gain

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